

What is claimed is :

1. A frame synchronous pattern processing
5 apparatus comprising:

a data switch section for performing a data
rearrangement processing of parallel data obtained
by serial/parallel conversion of multiplexed serial
10 data having a frame synchronous pattern based on an
SDH transmission system so that said frame
synchronous pattern is leading one;

a temporary region detection section for
temporarily detecting a candidate of region data
15 which may contain said frame synchronous pattern from
said parallel data and for serializing said temporary
region data;

a frame synchronous pattern detection section
for detecting said frame synchronous pattern from
20 said temporary region data obtained by said temporary
region detection section; and

a data switch control section for controlling
said data rearrangement processing by said data
switch section according to the detection state of
25 said temporary region data by said temporary region
detection section and to the detection state of said
frame synchronous pattern by said frame synchronous

pattern detection section.

2. A frame synchronous pattern processing apparatus according to claim 1:

5 wherein said temporary region detection section comprises :

 a temporary position information detection section for detecting temporary position information of said frame synchronous pattern in said
10 parallel data; and

 a temporary region data hold section for serially holding a given region parallel data including a reference position based on said temporary position information detected by said
15 temporary position information detection section as said temporary region data by turns and serially outputting said parallel data.

3. A frame synchronous pattern processing apparatus according to claim 2 :

 wherein said temporary position information detection section comprises :

 an A1 byte detection section for detecting an A1 byte from said parallel data;

25 an A2 byte detection section for detecting an A2 byte from said parallel data; and

 a switching control section for switching the

detection operations of said A1 byte detection section and said A2 byte detection section in response to the detection timing of said A1 byte and A2 byte;

5 in which the detection position of said A2 byte is supplied to said temporary region data hold section as said temporary position information when said A2 byte is detected in said A2 byte detection section after the detection of said A1 byte in said
10 A1 detection section by the switching operation of said switching control section.

4. A frame synchronous pattern processing apparatus according to claim 3 :

15 wherein said A1 byte detection section is composed to detect one byte of said A1 byte for each A1 byte leading position which may exist in said parallel data;

 and said A2 byte detection section is composed
20 to detect one byte of said A2 byte for each A2 byte leading position which may exist in said parallel data.

5. A frame synchronous pattern processing
25 apparatus according to claim 3 :

 wherein said switching control section comprises a control section for stopping said

8. A frame synchronous pattern processing apparatus according to claim 7 :

wherein said invalidation processing section
5 is composed to compare the leading position of said A1 byte detected in said A1 byte detection section and the leading position of said A2 byte detected in said A2 byte detection section, to determine said temporary region data invalid when respective
10 leading positions are different, and to perform said invalidation processing.

9. A frame synchronous pattern processing apparatus according to claim 8 :

15 wherein said invalidation processing section comprises an A1 byte leading position hold section for temporarily holding the leading position of said A1 byte detected in said A1 byte detection section; and

20 a comparison section for comparing the leading position of said A1 byte held in said A1 byte leading position hold section and the leading position of said A2 byte detected in said A2 byte detection section ;

25 in which said invalidation processing section is composed to determine said temporary region data invalid when the leading position of said A1 byte and

the leading position of said A2 byte are determined different through the comparison in said comparison section and to perform said invalidation processing.

5 10. A frame synchronous pattern processing apparatus according to claim 7 :
wherein said invalidation processing section comprises a timer for counting a given period of time upon the detection of said A1 byte in said A1 byte
10 detection section; and said invalidation processing section is composed to determine said temporary region data invalid when said A2 byte is not detected in said A2 byte detection section until the end of the counting operation of said timer and to perform
15 said invalidation processing.

11. A frame synchronous pattern processing apparatus according to claim 7 :

20 wherein said invalidation processing section comprises an A1 byte continuity monitoring section for monitoring if said A1 byte is continuously detected in said A1 byte detection section; and

25 said invalidation processing section is composed to determine said temporary region data invalid when the continuity of said A1 byte is not confirmed in said A1 byte continuity monitoring section and said A2 byte is not detected in said A2

byte detection section, and to perform said invalidation processing.

12. A frame synchronous pattern processing
5 apparatus according to claim 2 :

wherein said temporary position information detection section comprises ;

an A1/A2 byte detection section for
simultaneously detecting said A1 byte and said A2
10 byte from a plurality of time slots of said parallel data, and

when said A1 byte and said A2 byte are simultaneously detected in said A1/A2 byte detection section, said temporary position information
15 detection section supplies the detection position to said temporary region data hold section as said temporary position information.

13. A frame synchronous pattern processing
20 apparatus according to claim 2 :

wherein said temporary region data hold section comprises :

a plurality of shift stages having, according to the parallel factor of said parallel data,
25 multiple stages of shift circuits for temporary holding and shifting input data; and when said temporary position information is detected in said

temporary position information detection section,
said temporary region data hold section serializes
parallel input data by sequentially connecting the
output from the shift circuit of the lower stage side
5 in said shift stages to the input of the shift circuit
of the higher stage side and, by connecting the output
from the shift circuit of the highest stage in said
shift stages to the input of the shift circuit of the
lowest stage of following shift stages.

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14. A frame synchronous pattern processing
apparatus according to claim 2 further comprising a
mask processing section for masking the output from
said temporary region data hold section upon the
15 input of parallel data except said temporary region
data.

15. A frame synchronous pattern processing
apparatus according to claim 1 :

20 wherein said frame synchronous pattern
detection section is composed to perform said frame
synchronous pattern detection using serialization
processing of said temporary region data in
cooperation with said temporary region detection
25 section.

16. A frame synchronous pattern processing

apparatus according to claim 1 :

wherein said data switch control section is composed to generate as a control signal for said data switch section a data shift amount corresponding to the period of time from the detection of said temporary region data in said temporary region detection section to the detection of said frame synchronous pattern in said frame synchronous pattern detection section.

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17. A frame synchronous pattern processing apparatus according to claim 16 :

wherein said data switch control section comprises a counter for counting the count value corresponding to the number of parallels of said parallel data upon the detection of said temporary region data in said temporary region detection section ; and said data switch control section is composed to supply as said data shift amount to said data switch section the counted value of said counter at the time when said frame synchronous pattern is detected in said frame synchronous pattern detection section.

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18. A frame synchronous pattern detection apparatus comprising :

a temporary region detection section for

temporarily detecting a candidate of region data which may contain a frame synchronous pattern from multiplex data including said frame synchronous pattern based on a SDH transmission system; and

5 a frame synchronous pattern detection section for detecting said frame synchronous pattern from said temporary region data detected in said temporary region detection section.

10 19. A frame synchronous pattern detection apparatus comprising :

 a temporary region detection section for temporarily detecting a candidate of region data which may contain a given frame synchronous pattern
15 from data including said frame synchronous pattern; and

 a frame synchronous pattern detection section for detecting said frame synchronous pattern from said temporary region data detected in said temporary
20 region detection section.

 20. A frame synchronous pattern detection method apparatus for temporarily detecting a candidate of region data which may contain a given
25 frame synchronous pattern from data including said frame synchronous pattern, and for detecting said frame synchronous pattern from said temporary region

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data.